IN THE SPECIFICATION

Please replace the paragraph beginning on page 3, line 20, with the following paragraph:

A tunnel oxide layer 56 having a thickness of, for example, between approximately 80 and 130 [']Å separates a floating gate 54 for FG transistor 40a from n-well region 42. When floating gate 54 is negatively charged with respect to n-well region 42, a hole-containing channel region 52 is induced in n-well region 42. A similar channel region 53 may be induced for SG transistor 40b so that it functions as an enhancement-type transistor.